



Novel Three-Dimensional Vertical Interconnect Technology for Microwave and RF Applications

Kavita Goverdhanam
University of Michigan, Ann Arbor, Michigan

Rainee N. Simons
Dynacs, Inc., Brook Park, Ohio

Linda P.B. Katehi
University of Michigan, Ann Arbor, Michigan

The NASA STI Program Office . . . in Profile

Since its founding, NASA has been dedicated to the advancement of aeronautics and space science. The NASA Scientific and Technical Information (STI) Program Office plays a key part in helping NASA maintain this important role.

The NASA STI Program Office is operated by Langley Research Center, the Lead Center for NASA's scientific and technical information. The NASA STI Program Office provides access to the NASA STI Database, the largest collection of aeronautical and space science STI in the world. The Program Office is also NASA's institutional mechanism for disseminating the results of its research and development activities. These results are published by NASA in the NASA STI Report Series, which includes the following report types:

- **TECHNICAL PUBLICATION.** Reports of completed research or a major significant phase of research that present the results of NASA programs and include extensive data or theoretical analysis. Includes compilations of significant scientific and technical data and information deemed to be of continuing reference value. NASA's counterpart of peer-reviewed formal professional papers but has less stringent limitations on manuscript length and extent of graphic presentations.
- **TECHNICAL MEMORANDUM.** Scientific and technical findings that are preliminary or of specialized interest, e.g., quick release reports, working papers, and bibliographies that contain minimal annotation. Does not contain extensive analysis.
- **CONTRACTOR REPORT.** Scientific and technical findings by NASA-sponsored contractors and grantees.

- **CONFERENCE PUBLICATION.** Collected papers from scientific and technical conferences, symposia, seminars, or other meetings sponsored or cosponsored by NASA.
- **SPECIAL PUBLICATION.** Scientific, technical, or historical information from NASA programs, projects, and missions, often concerned with subjects having substantial public interest.
- **TECHNICAL TRANSLATION.** English-language translations of foreign scientific and technical material pertinent to NASA's mission.

Specialized services that complement the STI Program Office's diverse offerings include creating custom thesauri, building customized data bases, organizing and publishing research results . . . even providing videos.

For more information about the NASA STI Program Office, see the following:

- Access the NASA STI Program Home Page at <http://www.sti.nasa.gov>
- E-mail your question via the Internet to help@sti.nasa.gov
- Fax your question to the NASA Access Help Desk at (301) 621-0134
- Telephone the NASA Access Help Desk at (301) 621-0390
- Write to:
NASA Access Help Desk
NASA Center for Aerospace Information
7121 Standard Drive
Hanover, MD 21076

NASA/TM—1999-209043



Novel Three-Dimensional Vertical Interconnect Technology for Microwave and RF Applications

Kavita Goverdhanam
University of Michigan, Ann Arbor, Michigan

Rainee N. Simons
Dynacs, Inc., Brook Park, Ohio

Linda P.B. Katehi
University of Michigan, Ann Arbor, Michigan

Prepared for the
MTT-S International Microwave Symposium
sponsored by the Institute of Electrical and Electronics Engineers
Anaheim, California, June 13-19, 1999

National Aeronautics and
Space Administration

Glenn Research Center

March 1999

Acknowledgments

The authors are grateful to ONR (N00014-95-1-0546) for its support.

Available from

NASA Center for Aerospace Information
7121 Standard Drive
Hanover, MD 21076
Price Code: A02

National Technical Information Service
5285 Port Royal Road
Springfield, VA 22100
Price Code: A02

NOVEL THREE-DIMENSIONAL VERTICAL INTERCONNECT TECHNOLOGY FOR MICROWAVE AND RF APPLICATIONS

Kavita Goverdhanam¹, Rainee N. Simons², and Linda P.B. Katehi¹

¹Radiation Laboratory, EECS Department, University of Michigan,
Ann Arbor, Michigan 48109-2122

²NASA, Glenn Research Center, Dynacs Group, Cleveland, Ohio 44135

Abstract—In this paper, novel 3D interconnects suitable for applications in microwave and RF integrated circuit technology have been presented. The interconnect fabrication process and design details are presented. In addition, measured and numerically modeled results of the performance of the interconnects have been shown. The results indicate that the proposed technology has tremendous potential applications in integrated circuit technology.

I. INTRODUCTION

Recently, Microwave and RF integrated circuits (ICs) based on Silicon/Silicon germanium device technology have emerged as a viable alternative to ICs based on III-V semiconductor device technologies for wireless applications. These applications have experienced an exponential growth during the past few years. Current state-of-the-art digital ICs are also based on silicon technology and have the potential to be mono-lithically integrated with the above analogue ICs. Therefore, it is apparent that future generation of silicon analog circuits would have integrated digital control functions to enable them to make intelligent decisions. These advanced silicon mixed signal ICs would require efficient interconnects to allow combining different transmission media, such as, Coplanar Stripline (CPS) and Coplanar Waveguide (CPW) for maximum design flexibility. In addition, they are useful for enhancing packing density in the vertical direction as in small hand held communication devices. The interconnects have to be small in size for low parasitic coupling capacitances, and simple to fabricate for high yield and low manufacturing cost.

In this paper, we present several new design concepts for three-dimensional (3D) interconnects on a high resistivity (HR) silicon ($\epsilon_{r2} = 11.7$) wafer. The 3D interconnects constitute very small sections of CPS at two levels connected by metallized vias and separated by a thin layer of spin-on-glass (SOG). CPS has the advantages of eliminating backside processing due to its uniplanar construction, and greatly simplifying vertical integration by the use of metallized vias. In addition, CPS being a slot type of transmission line allows easy integration of other transmission media, such as, slotline, CPW with finite width ground planes and micro-CPS [1] for greater design flexibility. The SOG has the advantage of low dielectric constant ($\epsilon_{r1} = 3.1$) and hence low parasitic coupling capacitance. In addition, the SOG also planarizes the circuit and this

facilitates vertical integration [1]. The HR silicon wafer ($\rho > 3000\Omega\text{-cm}$) has the advantage of lowering the signal attenuation in addition to improving the isolation between adjacent circuits.

In the following sections, first, the fabrication process of vertical interconnects is presented. Next, design considerations for the CPS vertical interconnects treated here are presented. The interconnects that are presented here are: CPS vertically interconnected overpass with a crossover, a CPS vertical interconnect with 180° phase shift and a CPW vertical interconnect with 180° phase shift. Last, in the section on results and discussion, first, the measured loss for CPS lines on HR Silicon is presented. Second, the computed results showing the performance of the CPS vertically interconnected overpass with a crossover is presented. The Finite Difference Time Domain (FDTD) [2] technique has been used to compute the performance of the CPS vertically interconnected overpass with a crossover. Finally, the measured phase characteristics of the CPS and CPW interconnects with 180° phase shift are presented. The experimental work for the purpose of demonstrating the low loss feature of the interconnects was performed using RT/duroid. The fabrication and characterization of interconnects with SOG-on-HR silicon are currently in progress. It is interesting to note that the measured and FDTD simulated results indicate that the interconnects presented here exhibit very good performance over a broad range of frequencies.

II. INTERCONNECT FABRICATION

To begin the fabrication process, the lower strip conductor of thickness $t_1 = 0.8 \mu\text{m}$ is fabricated on the HR Silicon substrate by a lift-off process [3]. Next, the dielectric spacer layer is built-up to the required thickness by multiple spin-coats. Accuglass 512 SOG [4] is used as the dielectric spacer layer. The thickness h_1 of the Accuglass 512 SOG used here is $2.0 \mu\text{m}$. Lastly, the upper strip conductor of thickness $t_2 = 2.0 \mu\text{m}$ is fabricated using the lift-off process once again. Gold metallization is used for the conductors.

III. DESIGN CONSIDERATIONS

(a) CPS vertically interconnected overpass with crossover:
A CPS vertically interconnected overpass with a crossover on a HR silicon wafer of thickness $h_2 = 400 \mu\text{m}$ is

shown in Figure 1. In this interconnect, the CPS strip width $W_1 = W_2 = W$ and the separations $S_1 = S_2 = S$ are chosen such that the characteristic impedance $Z_{o(\text{CPS})}$ is 50Ω . The thickness of the SOG layer is h_1 . The vertical interconnection between the first and the second level CPS conductors are provided by a pair of circular metallized vias. Each via in a pair is symmetrically located on the strip conductor and has a diameter d . A via pair is design as a small section of a vertical balanced transmission line with characteristic impedance $Z_{o(\text{via})} = 50\Omega$. The $Z_{o(\text{via})}$ is related to the diameter d , separation between vias in a pair S_4 and the dielectric constant of the medium surrounding the via ϵ_{r1} through the expression, $Z_{o(\text{via})} = (60/\text{sqrt}(\epsilon_{r1}))\cosh^{-1}(N)$, where $N = 0.5[(2S_4/d)^2 - 2]$. The probe pad at the input and output for the characterization with microwave wafer probes is typically about $100\ \mu\text{m} \times 100\ \mu\text{m}$ in size.

(b) CPS Vertical Interconnect with 180° phase shift:

A CPS 180° phase shifter with vertically interconnected twisted overpass is shown in Figure 2. In this phase shifter, the CPS strip width W and separation S are chosen such that the characteristic impedance $Z_{o(\text{CPS})}$ is 50Ω . The via diameter d is chosen to be the same as in Figure 1.

(c) CPW Vertical Interconnect with 180° phase shift:

A CPW 180° Phase shifter with vertically interconnected U-shaped overpass is shown in Figure 3. In this phase shifter, the CPW center strip conductor and slot widths S and W are chosen such that the characteristic impedance $Z_{o(\text{CPW})}$ is 50Ω . The via diameter is chosen to be the same as in Figure 1.

IV. RESULTS AND DISCUSSION

(a) Measured Loss of CPS on HR Silicon:

In order to estimate the efficiency of the interconnects, the loss per unit length for 50Ω CPS is measured for a range of CPS test structures with W ranging from 26 to $133\ \mu\text{m}$ and S ranging from 2 to $10\ \mu\text{m}$. This range presents typical dimensions encountered in practical circuits. In Figure 4, the measured loss is presented as a function of W and frequency. As an example, for a CPS with $W = 54\ \mu\text{m}$ and $S = 4\ \mu\text{m}$, the measured loss is of the order of $0.46\ \text{dB/mm}$. The CPS crossover in Figure 1 has a length of about $328\ \mu\text{m}$ between the via pairs and hence the loss is estimated to be about $0.15\ \text{dB}$ at $20\ \text{GHz}$. However, instead of choosing such small dimension, if S is chosen to be larger, say $10\ \mu\text{m}$, the corresponding loss for a 50Ω line reduces to about $0.25\ \text{dB/mm}$, roughly reducing the total loss of the CPS crossover to about $0.075\ \text{dB}$ at $20\ \text{GHz}$.

(b) CPS vertically interconnected overpass with crossover:

In order to study the performance of this interconnect, the scattering parameters (S-parameters) were computed using the FDTD scheme and they are shown in Figure 5.

The computed S-parameters for the overpass alone indicate that the insertion loss, (S_{21}) is negligible and that the return loss (S_{11}) is about $-28\ \text{dB}$. The computed S-parameters for the overpass with a crossover shows that the insertion loss is still very small. However, S_{11} has increased from $-28\ \text{dB}$ to $-12\ \text{dB}$. This increase in S_{11} can be offset by providing a step compensation as shown in Figure 1. Simulations with the step compensation are in progress. Computed S_{31} shows that the coupling between the overpass and the crossover is less than $-40\ \text{dB}$.

(c) CPS and CPW vertical interconnects with 180° Phase Shift:

The measured phase characteristics for these circuits are shown in Figures 6 and 7. In these figures, the phase shift of the interconnect is compared with the phase of an equivalent length of through-line. From the figures, it is observed that the phase shift of the interconnect is close to 180° over a very broad range of frequencies. The excess loss of the interconnect is close to $0.1\ \text{dB}$. FDTD simulations of the phase shifters are in progress.

V. CONCLUSION

A new 3D interconnect technology suitable for applications in microwave and RF integrated circuits has been proposed. Small sections of Coplanar Striplines connected by metallized vias and separated by a thin layer of spin-on-glass have been used to realize a variety of broadband high performance circuits. This technology yields small sized interconnects which are simple to fabricate. As examples, the CPS vertically interconnected overpass with a crossover, and 180° CPS and CPW phase shifters have been presented. The results obtained indicate the suitability of the proposed approach in facilitating 3D integration.

REFERENCES

1. K. Goverdhanam, R.N. Simons and L.P.B. Katehi, "Micro-Coplanar Striplines—new transmission Media for Microwave Applications," 1998 IEEE MTT-S Inter. Microwave Symp., Dig., Vol. 2, Baltimore, Maryland, pp. 1035–1038, 1998.
2. K. Goverdhanam, R.N. Simons and L.P.B. Katehi, "Coplanar Stripline Components for High-Frequency Applications," IEEE Trans. on Microwave Theory and Techniques, Vol. 45, No. 10, pp. 1725–1729, Oct. 1997.
3. R. Williams, "Modern GaAs processing Methods," 2nd ed., Ch. 6, Norwood, MA: Artech House Inc. 1990.
4. Accuglass® 512 Spin-on-Glass (SOG), Product Bulletin, Allied-Signal Inc., Planarization and diffusion products, 1090 S. Milpitas Blvd., Milpitas CA 95035.

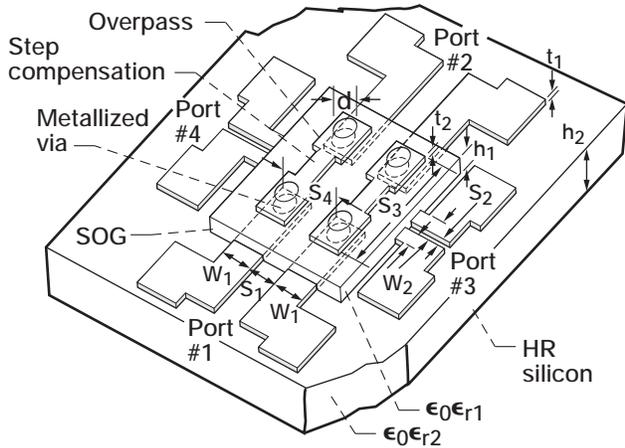


Figure 1.—Geometry of CPS overpass with crossover
 $W_1 = W_2 = W = 54 \mu\text{m}$ $S_1 = S_2 = S = 4 \mu\text{m}$, $d = 45 \mu\text{m}$,
 $S_3 = 328 \mu\text{m}$, $S_4 = 58 \mu\text{m}$.

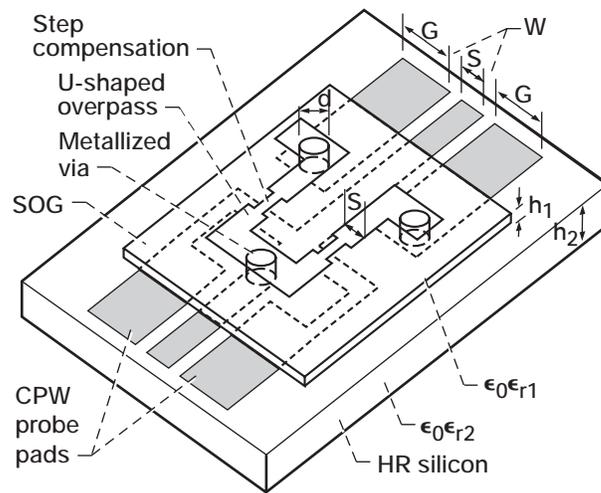


Figure 3.—CPW vertical interconnect with 180° phase shift
 $S = 54 \mu\text{m}$, $W = 34 \mu\text{m}$, $G = 239 \mu\text{m}$.

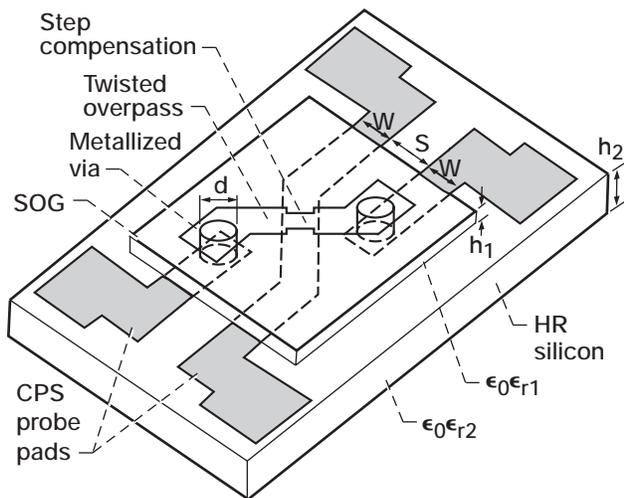


Figure 2.—CPS vertical interconnect with 180° phase shift
 $W = 54 \mu\text{m}$, $S = 4 \mu\text{m}$.

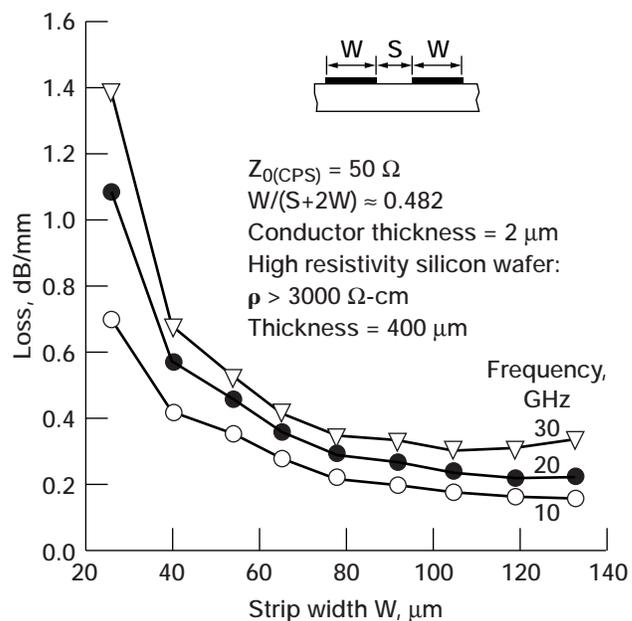


Figure 4.—Measured CPS loss versus strip width.

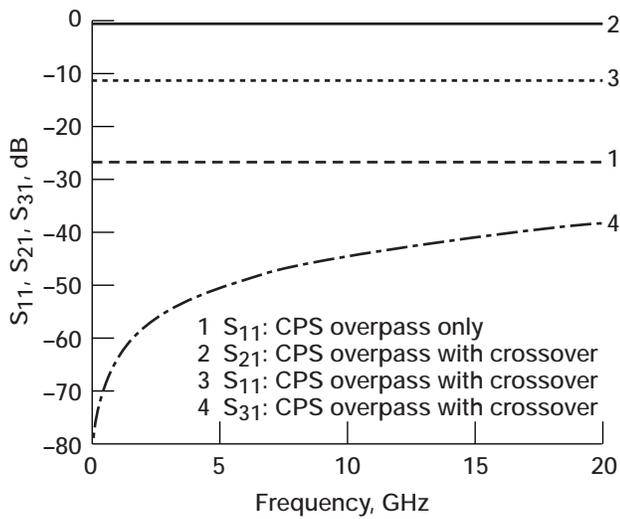


Figure 5.—Computed S-parameters for CPS vertically interconnected overpass with crossover.

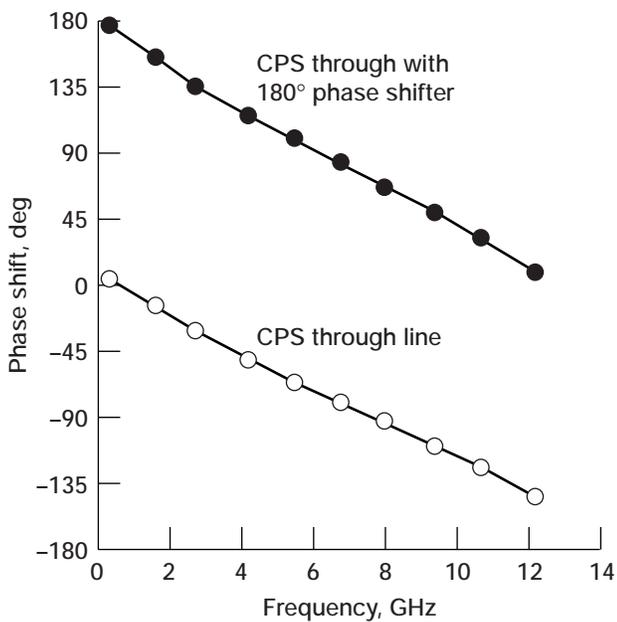


Figure 6.—Measured phase shift versus frequency $h_2 = 254 \mu\text{m}$, $\epsilon_{r2} = 10.5$, $W = 254 \mu\text{m}$, $S = 75 \mu\text{m}$.

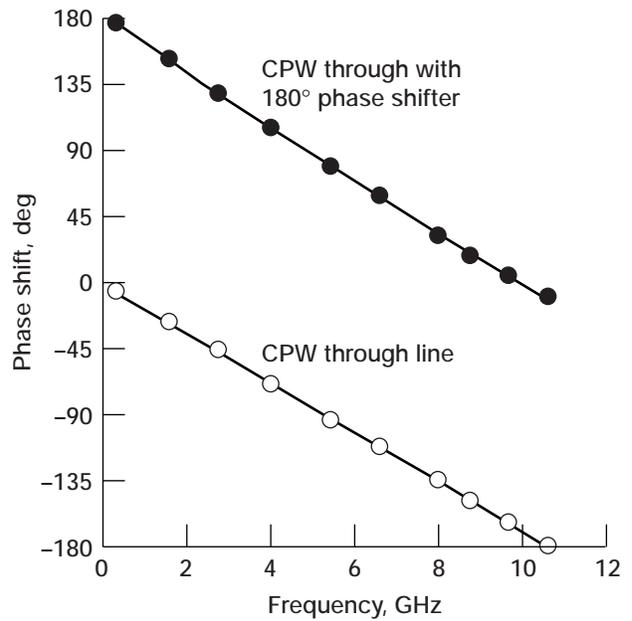


Figure 7.—Measured phase shift versus frequency $h_2 = 254 \mu\text{m}$, $\epsilon_{r2} = 10.5$, $S = 165 \mu\text{m}$, $W = 75 \mu\text{m}$, $G = 457 \mu\text{m}$.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (<i>Leave blank</i>)		2. REPORT DATE March 1999	3. REPORT TYPE AND DATES COVERED Technical Memorandum	
4. TITLE AND SUBTITLE Novel Three-Dimensional Vertical Interconnect Technology for Microwave and RF Applications			5. FUNDING NUMBERS WU-632-50-5B-00	
6. AUTHOR(S) Kavita Goverdhanam, Rainee N. Simons, and Linda P.B. Katehi				
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) National Aeronautics and Space Administration John H. Glenn Research Center at Lewis Field Cleveland, Ohio 44135-3191			8. PERFORMING ORGANIZATION REPORT NUMBER E-11573	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) National Aeronautics and Space Administration Washington, DC 20546-0001			10. SPONSORING/MONITORING AGENCY REPORT NUMBER NASA TM-1999-209043	
11. SUPPLEMENTARY NOTES Prepared for the MTT-S International Microwave Symposium sponsored by the Institute of Electrical and Electronics Engineers, Anaheim, California, June 13-19, 1999. Kavita Goverdhanam and Linda P.B. Katehi, University of Michigan, Radiation Laboratory, EECS Department, Ann Arbor, Michigan 48109-2122; Rainee N. Simons, Dynacs, Inc., 2001 Aerospace Parkway, Brook Park, Ohio 44142 (work funded by NASA Contract NAS3-98008). Responsible person, Rainee N. Simons, organization code 5640, (216) 433-3462.				
12a. DISTRIBUTION/AVAILABILITY STATEMENT Unclassified - Unlimited Subject Category: 33 This publication is available from the NASA Center for AeroSpace Information, (301) 621-0390.			12b. DISTRIBUTION CODE	
13. ABSTRACT (<i>Maximum 200 words</i>) In this paper, novel 3D interconnects suitable for applications in microwave and RF integrated circuit technology have been presented. The interconnect fabrication process and design details are presented. In addition, measured and numerically modeled results of the performance of the interconnects have been shown. The results indicate that the proposed technology has tremendous potential applications in integrated circuit technology.				
14. SUBJECT TERMS Coplanar stripline; Vertical interconnect; Spin-on-glass; High resistivity silicon; Antennas			15. NUMBER OF PAGES 10	
			16. PRICE CODE A02	
17. SECURITY CLASSIFICATION OF REPORT Unclassified	18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT	